MX370001A TD-SCDMA Waveform Pattern Operation Manual

Third Edition

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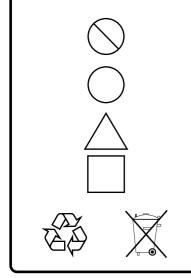
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This indicates a note. The contents are described in the box.

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MX370001A **TD-SCDMA Waveform Pattern Operation Manual**

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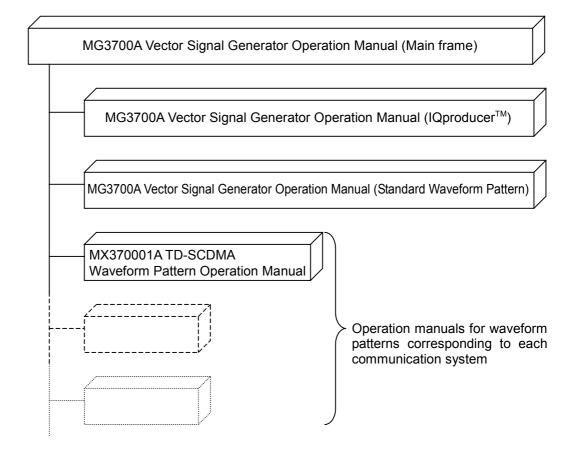
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About This Manual

Composition of Operation Manuals

The operation manuals for the MG3700A Vector Signal Generator are comprised as shown in the figure below. Read them when needed in addition to this manual.



Scope of This Manual

This manual mainly describes how to use the waveform patterns included in the MX370001A TD-SCDMA Waveform Pattern that can be used in the arbitrary waveform generators integrated in the MG3700A Vector Signal Generator, the detailed specifications for each waveform pattern are given as well. Detailed information about the TD-SCDMA waveform patterns is described in Section 3 "Details of Waveform Pattern."

The detailed operation method of the waveform pattern in the MG3700A Vector Signal Generator is described in the MG3700A Operation Manual (Mainframe). Read it in conjunction with this manual.

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Section 1 Outline

This section provides an outline of the product and describes the standard product composition for the MX370001A TD-SCDMA Waveform Pattern.

1.1	Outline of Product	1-2
1.2	Product Composition	1-3

1.1 Outline of Product

The MX370001A TD-SCDMA Waveform Pattern (hereafter referred to as "MX370001A") includes standard waveform patterns that are prescribed in 3GPP TD-SCDMA (1.28 Mcps TDD Option).

The TD-SCDMA waveform patterns are classified broadly into the following signals:

- Downlink signals for BS transmitter tests: Used to evaluate the devices used by the BS.
- Uplink signals for BS receiver tests: Used to evaluate the reception systems such as BS reception sensitivity measurement.
- Downlink signals for UE receiver tests:

Used to evaluate the reception systems such as UE reception sensitivity measurement.

Waveform patterns included in the MX370001A can be output as modulated signals by downloading them to the MG3700A Vector Signal Generator (hereafter referred to as "MG3700A") that integrates an arbitrary waveform pattern generator.

Note:

The waveform pattern described here indicates arbitrary waveform data used for supporting various radio communication systems that can be used by the arbitrary waveform generator integrated in the MG3700A.

The waveform pattern consists of two files: arbitrary waveform file and waveform information file. The arbitrary waveform file is a binary-format file with the extension ".wvd". The waveform information file is a text-format file with the extension ".wvi", used to control arbitrary waveform data and set the hardware for waveform data output.

A license for the MX370001A must be purchased that matches the serial number of the MG3700A to be used. When using the MX370001A with two or more MG3700A units, purchase the license for the MX370001A for the number of the MG3700A units to be used.

1.2 Product Composition

Table 1.2-1 below lists the product composition of the MX370001A. After opening the package, confirm that all the products listed below are included in the box. If anything is missing or damaged, contact Anritsu Corporation or one of its distributors.

ltem	Model/No.	Product	Q'ty	Remarks
Main unit	MX370001A	TD-SCDMA Waveform Pattern	1	Provided in two DVDs. The license file and operation manual file are included.

Table 1.2-1 Product composition

Section 1 Outline

Section 2 How to Use Waveform Pattern

This section describes how to use the MX370001A.

2.1 How to Use Waveform Pattern 2-2

2.1 How to Use Waveform Pattern

The MX370001A is shipped in two DVDs.

The following shows the procedure to output modulated signals from the MG3700A by using the MX370001A:

<Procedure>

- 1. Install the MX370001A license file (MX370001A.key) stored in the DVD into the MG3700A to be used.
- 2. Transfer the waveform pattern stored in the DVD to the MG3700A internal hard disk.
- 3. Load the waveform pattern transferred and saved in the MG3700A internal hard disk to an arbitrary waveform memory.
- 4. Select the waveform pattern loaded in the arbitrary waveform memory as an output waveform pattern.

Refer to Section 3.9.9 "Installation" in the MG3700A Operation Manual (Main frame) or Section 5.1 "Installing License File" in the MG3700A Operation Manual (IQproducerTM) for how to install the license file.

There are two methods for transferring waveform patterns to the MG3700A internal hard disk: using a compact flash card and via LAN.

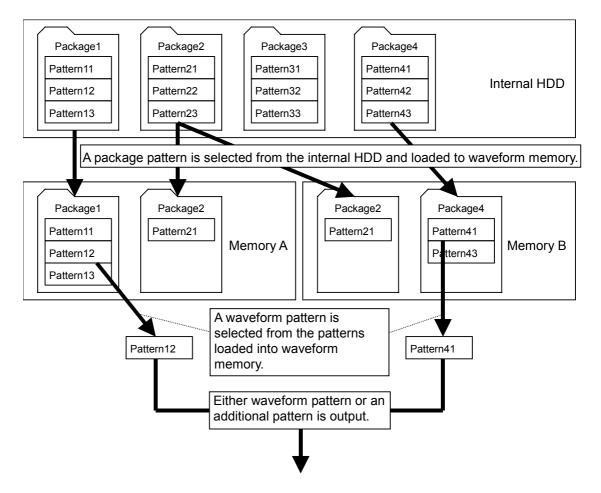
Refer to Section 3.5.2 "Using waveform pattern for modulation" in the MG3700A Operation Manual (Mainframe) for details of the transfer method using a compact flash card.

Refer to Section 4.6 "File Transfer and Loading to Memory in Transfer & Setting Panel Screen" in the MG3700A Operation Manual (IQproducerTM) for details of the transfer method via LAN.

The operational outlines for the loading of the waveform patterns stored in the internal hard disk to an arbitrary waveform memory and waveform pattern selection are provided below.

Waveform patterns are classified by communication type and are stored in a folder. This folder is called a "package." The MX370001A are stored in the "TD-SCDMA (MX370001A)" package. When reproducing a waveform pattern, it is necessary first to load the package pattern stored in the internal hard disk to a waveform memory in the MG3700A. The MG3700A has two waveform memories A and B that have the I/Q 2-channel configuration. Waveform patterns are loaded to either or both of these two waveform memories.

Then, select a waveform pattern to be output from the patterns loaded into the waveform memory. Only one waveform pattern can be selected from each memory. A waveform pattern is selected from waveform memory A or B, or an additional waveform is generated by adding the two waveform patterns selected from both waveform memories A and B to be output.



Refer to Section 3.5.2 "Using waveform pattern for modulation" in the MG3700A Operation Manual (Mainframe) for details on waveform pattern selection.

Section 3 Details of Waveform Pattern

This section describes details of the MX370001A, the trigger function, and auxiliary signal output.

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- 3.3 External Trigger Function 3-14
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3.1 Waveform Pattern Types

The MX370001A includes the following standard TD-SCDMA waveform patterns that conform to the 3GPP standard.

To at Townsh		UE	Receiver Test	(DL)					
Test Target	UE								
Test Signal	UE-DL RMC								
Waveform Pattern	rmc12_2k _ue_dl	rmc12k_ ocns_ ue_dl	rmc64k_ ocns_ ue_dl	rmc144k_ ocns_ ue_dl	rmc384k_ ue_dl				
Reference Standard			TS25.102						
DwPTS/UpPTS SYNC_DL/UL NUMBER (quadruples)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)				
P-CCPCH	Add	Add	Add	Add	Add				
Scrambling Code	0	0	0	0	0				
midamble ID	0	0	0	0	0				
Maximum User (user number)	8 (1)	8 (1)	8 (1)	8 (1)	8 (1)				
Spreading Factor	16	16	16	16	16				
TimeSlot Number	4	4	4	4,5	3, 4, 5, 6				
Number of DPCH0	0	8	2	2	0				
DPCH Channelization Codes	C (i, 16) i = 1, 2	C (i, 16) i = 1, 2	C (i, 16) i = 1,, 8	C (i, 16) i = 1,, 8	C (i, 16) i = 1,, 10				
DPCH0 Channelization Codes	_	C (i, 16) $3 \le i \le 10$	C (i, 16) $9 \le i \le 10$	C (i, 16) $9 \le i \le 10$	_				
Data: DPCH0	PN9	PN9	PN9	PN9	PN9				
Data: other channel	P-CCPCH [*]	P-CCPCH [*]	P-CCPCH [*]	P-CCPCH [*]	P-CCPCH [*]				
Σ DPCH_Ec/Ior [dB]	0	-7	—						
DPCH0_Ec/Ior [dB]	_	-10	-10	-10	0				
DPCH Channelization Codes Power [dB]/1ch	-3.01	-10.00	-10.00	-10.00	-10				
DPCH0 Channelization Codes Power [dB]/1ch	_	-10.00	-10.00	-10.00	-				
IQ output level		\sqrt{I}	$r^2 + Q^2 = 320n$	ηV					

Table 3.1-1 List of TD-SCDMA waveform patterns for UE reception system evaluation

*: "Frame number/2" is inserted to the first 11 bits for P-CCPCH. The frame number is a repetition of 0, 1, 2, 3, 0, 1, 2, 3, ...

Toot Torget	BS Transmitter Test (DL)							
Test Target	BS							
Test Signal	BS-DL RMC							
Waveform Pattern	rmc– 1code _bs_dl	rmc– P-CCPCH _bs_dl	rmc– 8 code _bs_dl	rmc– 10 code _bs_dl				
Reference Standard		TS25	5.142					
DwPTS/UpPTS SYNC_DL/UL NUMBER (quadruples)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)	SYNC_DL #0 (S1)				
P-CCPCH	_	add	_	_				
Scrambling Code	0	0	0	0				
midamble ID	0	0	0	0				
Maximum User (user number)	2 (1)	8 (1)	2 (1)	2 (1)				
Spreading Factor	16	16	16	16				
TimeSlot Number	4, 5, 6	0	4, 5, 6	4, 5, 6				
Number of DPCH0	—	—	0	0				
DPCH Channelization Codes	C (i, 16) i = 1	_	C (i, 16) $1 \le i \le 8$	C (i, 16) 1 ≤ i ≤ 10				
DPCH0 Channelization Codes	—	—	—	—				
Data: DPCH0	$PN9^{*1}$	—	$PN9^{*1}$	$PN9^{*1}$				
Data: other channel	—	P-CCPCH ^{*2}	—	_				
Σ DPCH_Ec/Ior [dB]	0	—	0	0				
DPCH0_Ec/Ior [dB]								
DPCH Channelization Codes Power [dB]/1ch	0	_	-9	-10				
DPCH0 Channelization Codes Power [dB]/1ch	_	_	_	_				
IQ output level		$\sqrt{\mathbf{I}^2 + \mathbf{Q}^2}$	= 320mV					

Table 3.1-2 List of TD-SCDMA waveform patterns for BS transmission system evaluation

*1: 1-frame period data

*2: "Frame number/2" is inserted to the first 11 bits for P-CCPCH. The frame number is a repetition of 0, 1, 2, 3, 0, 1, 2, 3, ...

Section 3 Details of Waveform Pattern

Toot Townot	BS Receive Test (UL)								
Test Target	BS BS-UL RMC								
Test Signal									
Waveform Pattern	rmc12_2k rmc12k_ rmc64k_ _bs_ul _bs_ul _bs_ul _bs_ul			rmc144k rmc384 _bs_ul _bs_u					
Reference Standard			TS25.142						
DwPTS/UpPTS SYNC_DL/UL NUMBER (quadruples)	_	_	_	_	_				
P-CCPCH	—	—	_	_	-				
Scrambling Code	0	0	0	0	0				
midamble ID	0	0	0	0	0				
Maximum User (user number)	2 (1)	2 (1)	2 (1)	2 (1)	2 (1)				
Spreading Factor	8	8	2, 8	2, 8	8, 2				
TimeSlot Number	1	1	1	1, 2	1, 2, 3, 4				
Number of DPCH0	0	4	1	1	0				
DPCH Channelization Codes	C (i, 8) i = 1	C (i, 8) i = 1	C (i, 2) i = 1	C (i, 2) i = 1	$\begin{array}{c} C (i, 2) \\ i = 1 \\ C (i, 8) \\ i = 5 \end{array}$				
DPCH0 Channelization Codes	_	$\begin{array}{c} C \ (i, \ 8) \\ 2 \leq i \leq 5 \end{array}$	C (i, 8) i = 5	C (i, 8) i = 5	_				
Data: DPCH0	PN9	PN9	PN9	PN9	PN9				
Data: other channel	_	_	_	_	-				
Σ DPCH_Ec/Ior [dB]	0	_	-	-	0				
DPCH0_Ec/Ior [dB]	_	-7	-7	-7	_				
DPCH Channelization Codes Power [dB]/1ch	0	-7	-0.97	-0.97	C (i, 2) = -6.99 C (i, 8) = -0.97				
DPCH0 Channelization Codes Power [dB]/1ch	-	-7	-7	_7	-				
IQ output level		\sqrt{I}	$r^2 + Q^2 = 320 r$	nV					

Table 3.1-3 List of TD-SCDMA waveform patterns for BS reception system evaluation

3.2 Waveform Pattern Frame Format

This section shows the frame formats of the MX370001A and describes the settings in detail.

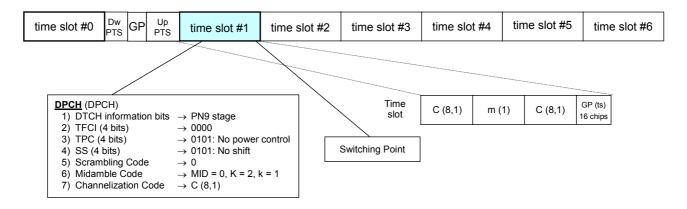
- ♦rmc12_2k_bs_ul
- For UE transmitter test (Uplink) TS25.102: UE UL reference measurement channel A.2.1.2, 1.28 Mcps, 12.2 kbps, SF = 8

Test Items: 6.2 Transmit power (Maximum output power) 6.3 UE frequency stability

- For BS receiver test (Uplink) TS25.142: BS UL reference measurement channel A2.1.2, 1.28 Mcps, SF = 8
 - Test Items: 7.2 Reference sensitivity level
 - 7.3 Dynamic range

7.4 Adjacent Channel Selectivity (ACS)

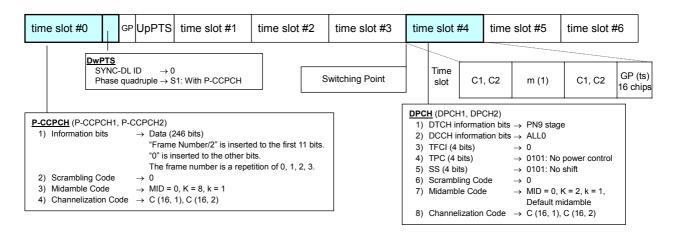
- 7.5 Blocking characteristics
- 7.6 Intermodulation characteristics



- rmc12_2k_ue_dl
- For UE receiver test (Downlink) TS25.102: UE DL reference measurement channel A.2.2.2.1, 1.28 Mcps, 12.2 kbps, SF = 16

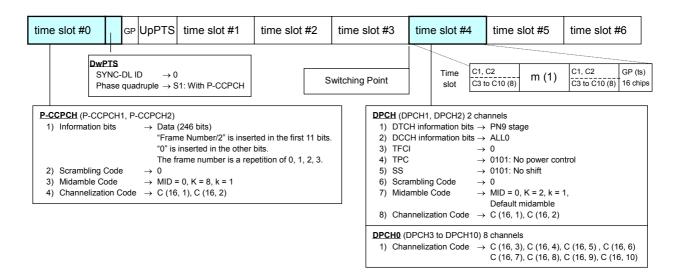
Test Items: 7.3 Reference sensitivity level

- 7.4 Maximum input level
 - 7.5 Adjacent Channel Selectivity (ACS)
 - 7.6 Blocking characteristics
 - 7.7 Spurious response
 - 7.8 Intermodulation characteristics



- rmc12k_ocns_ue_dl
- For UE receiver test (Downlink) TS25.102: UE DL reference measurement channel, A.2.2.2, 1.28 Mcps, (12.2 kbps), SF = 16

Test Items: 7.4 Maximum input level (Minimum Requirement) 8. Performance requirement (8.2.1.1.2 Table 8.2A)



- ♦ rmc64k_ocns_ue_dl
- For UE receiver test (Downlink) TS25.102: UE DL reference measurement channel A.2.3.2, 1.28 Mcps, (64 kbps), SF = 16

Test Items: 8. Performance requirement (8.2.1.1.2 Table 8.2A)

time slot #0		GΡ	UpPTS	time slot #1	time slot #2	time slot	t #3	tim	e slot #4	time slot #5	time slot #6
	NC-E			51: With P-CCPCH	5	witching Po	int		Time C1 t slot C9,	o C8 (8) C10 m (1)	C1 to C8 (8) GP (ts) C9, C10 16 chips
P-CCPCH (P-CCF 1) Information b 2) Scrambling (3) Midamble Cc 4) Channelization	oits Code ode			inserted in the other rame number is a rep = 0, K = 8, k = 1			1) 2) 3) ⁻ 4) ⁻ 5) 5 6) 5 7)	DTCH DCCH TFCI TPC SS Scram Midam	information bits bling Code ble Code	$\begin{array}{l} s \rightarrow {\sf PN9 \ stage} \\ s \rightarrow {\sf ALL0} \\ \rightarrow {\sf 0} \\ \rightarrow {\sf 0101: \ No \ power} \\ \rightarrow {\sf 0101: \ No \ shift} \\ \rightarrow {\sf 0} \\ \rightarrow {\sf MID} = {\sf 0, \ K} = 2, \\ {\sf Default \ midamb} \\ \rightarrow {\sf C} \left({\sf 16, \ 1} \right), {\sf C} \left({\sf 16} \right) \end{array}$	k = 1,
								•	CH9, DPCH10) elization Code	2 channels → C (16, 9), C (16	, 10)

- rmc144k_ocns_ue_dl
- For UE receiver test (Downlink)

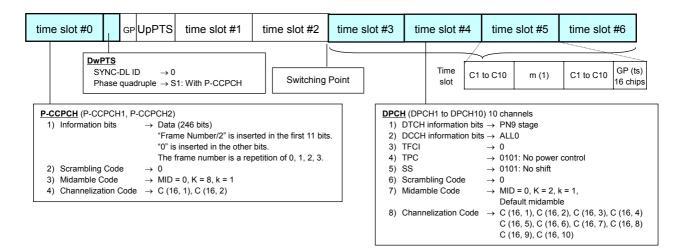
TS25.102: UE DL reference measurement channel A.2.4.2, 1.28 Mcps, (144 kbps), SF = 16

Test Items: 8. Performance requirement (8.2.1.1.2 Table 8.2A)

time slot #0	G	P UpPTS	time slot #1	time slot #2	time slot	t #3	time slot #4	time slot #5	time slot #6
	NC-D) S1: With P-CCPCH	s	witching Po	int		to C8 (8) C10 m (1)	C1 to C8 (8) GP (ts) C9, C10 16 chips
P-CCPCH (P-CCF 1) Information B		→ Data "Frar "0" is	(246 bits)			1) 2) 3) ⁻	<u>I</u> (DPCH1 to DPCH8) DTCH information bits DCCH information bits TFCI TPC	s \rightarrow PN9 stage	control
 2) Scrambling (3) Midamble Co 4) Channelizati 	ode		= 0, K = 8, k = 1 6, 1), C (16, 2)			6) 5 7) 1	SS Scrambling Code Midamble Code	→ 0101: No shift → 0 → MID = 0, K = 2, Default midamb	le
						DPCH	Channelization Code <u>1</u> (DPCH9, DPCH10) Channelization Code	C (16, 5), C (16 2 channels	, 2), C (16, 3), C (16, 4) , 6), C (16, 7), C (16, 8) , 10)

- ♦ rmc384k_ue_dl
- For UE receiver test (Downlink) TS25.102: UE DL reference measurement channel A.2.5.2, 1.28 Mcps, (384 kbps), SF = 16

Test Items: 8. Performance requirement (8.2.1.1.2 Table 8.2A)



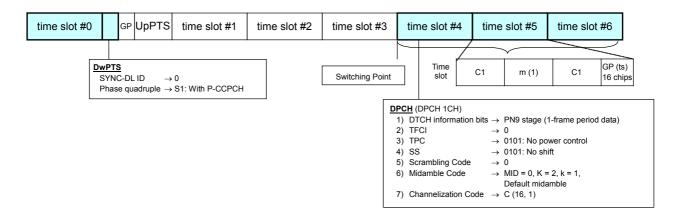
- rmc-8code_bs_dl
- For BS transmitter test (Downlink) TS25.142

Test Items: 6.2 Maximum Output power

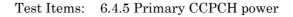
- 6.5 Transmit ON/OFF power
- 6.6 Output RF spectrum emission
- 6.7 Transmit Intermodulation

time slot #0	GP	UpPTS	time slot #1	time slot #2	time slot #3	tim	ne slot #4	time slot #5	time slot #6
	VC-DI		0 S1: With P-CCPCH			1) DT(2) TF(3) TP(4) SS 5) Scr 6) Mid	DPCH1 to DPCH CH information Cl C rambling Code damble Code	bits \rightarrow PN9 stage (1 \rightarrow None \rightarrow None \rightarrow None \rightarrow 0 \rightarrow MID = 0, K = Default mida de \rightarrow C (16, 1), C (2, k = 1,

- rmc-1code_bs_dl
- For BS transmitter test (Downlink) TS25.142: SF = 16
 - Test Items: 6.3 Frequency stability 6.4 Output power dynamics (Table 6.4A /Table 6.6A /1Code. Table 6.7A) 6.8 Transmit Modulation (Table 6.39C)

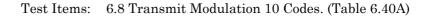


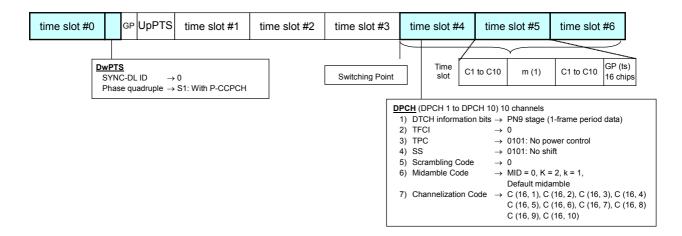
- ♦ rmc–P-CCPCH_bs_dl
- For BS transmitter test (Downlink) TS25.142: SF = 16



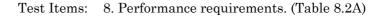
time slot #0 GP UpPTS time slot #1	time slot #2	time slot #3	time slot #4	time slot #5	time slot #6	6
$\frac{DwPTS}{SYNC-DL ID} \rightarrow 0$ Phase quadruple → S1: With P-CCPCH		Switching Point	Time slot	C1, C2 m (1)		GP (ts) 6 chips
P-CCPCH (P-CCPCH1, P-CCPCH2) 1) Information bits \rightarrow Data (246 bits) "Frame Number/2" is inserted "6" is inserted in the other bits 2) Scrambling Code \rightarrow 0 3) Midamble Code \rightarrow MID = 0, K = 8, k = 1 4) Channelization Code \rightarrow C (16, 1), C (16, 2)						

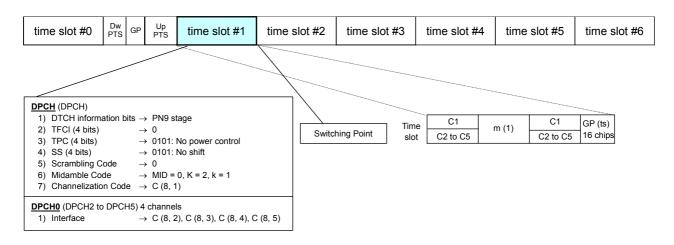
- ♦ rmc-10code_bs_dl
- For BS transmitter test (Downlink) TS25.142: SF = 16





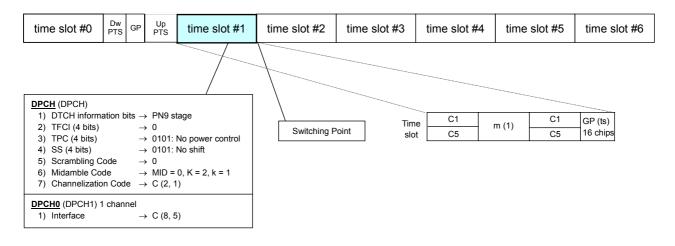
- rmc12k_ocns_bs_ul
- For BS receiver test (Uplink) TS25.142: BS UL reference measurement channel, A2.1.2, 1.28 Mcps, SF = 8





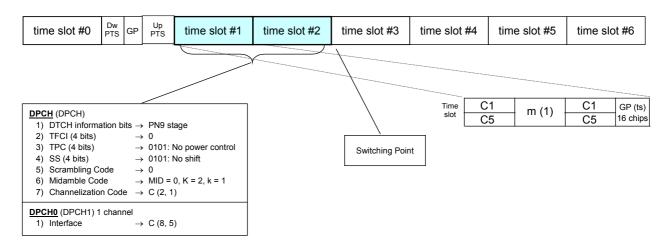
- ♦ rmc64k_ocns_bs_ul
- For BS receiver test (Uplink) TS25.142: BS UL reference measurement channel, A2.2.2, 1.28 Mcps, SF = 2, 8

Test Items: 8. Performance requirements. (Table	e 8.2A)
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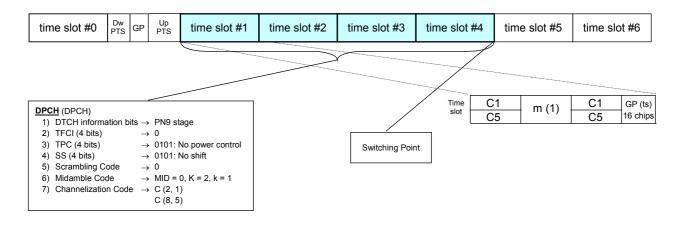
- rmc144k_bs_ul
- For BS receiver test (Uplink) TS25.142: BS UL reference measurement channel, A2.3.2, 1.28 Mcps, SF = 8

(Table 8.2A)
(



- rmc384k_bs_ul
- For BS receiver test (Uplink) TS25.142: BS UL reference measurement channel, A2.3.2, 1.28 Mcps, SF = 2, 8

Test Items:	8. Performance	requirements.	(Table 8.2A)
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3.3 External Trigger Function

Modulated signals can be output from the MG3700A in synchronization with an external trigger signal by using the external trigger function of the MG3700A. There are two external trigger functions as below. However, the frame trigger function cannot be used with the MX370001A.

- Start trigger function: Modulated signal output starts when a trigger signal is input for the first time in the trigger wait status, and signals are output continuously. The trigger delay function is provided.
 Frame trigger function: Cannot be used with the MX370001A. Modulated signal output starts when a trigger
 - wait status, and signal output starts when a trigger wait status, and signal output stops when signals in one frame have been output. After this, the MG3700A enters the trigger wait status, and repeats the operation above.

Refer to Section 3.5.4 "Outputting signal in sync with external trigger signal" in the MG3700A Operation Manual (Mainframe) for details of the external trigger function.

3.4 Auxiliary Signal Output

When using the MX370001A, the following auxiliary signals are output from the AUX Input/Output connectors on the rear panel of the MG3700A: Frame Clock (from Connector 1), Subframe Clock (from Connector 2), and RF Gate (from Connector 3).

• Frame Clock

As Frame Clock, a pulse is output in synchronization with the first symbol of a frame. The polarity of the signal can be inverted by changing Polarity of Marker1.

• Subframe Clock

As Subframe Clock, a pulse is output in synchronization with the first symbol of a subframe. The polarity of the signal can be inverted by changing Polarity of Marker2.

• RF Gate

When the used waveform pattern is burst, the RF Gate signal indicates the RF output burst ON/OFF status. The correspondence between the burst ON/OFF status and the output signal is as follows:

Burst ON: High level Burst OFF: Low level (The correspondence shown above is for the case when Polarity of Marker3 is Positive. It is inverted when Polarity is Negative.)

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